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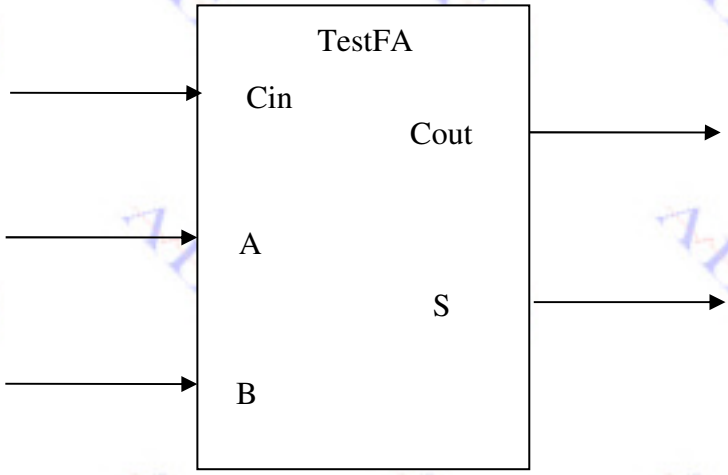
VHDL Architecture
Dataflow example

Create a design with the dataflow description which implements this truth table:

Inputs			Outputs	
Cin	A	B	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Create this model (named TestFA):



1. Implements this model with VHDL dataflow instructions.
2. Simulate and validate your design
3. Connect inputs on switch (of your choice) and outputs on LEDs. Download your design on the evaluation board. Check the result.
4. Does your design fit in the FPGA? What is the free space remaining?
5. What is the shortest path of your design (the faster one)? What is the critical path of your design (the slower one) ?