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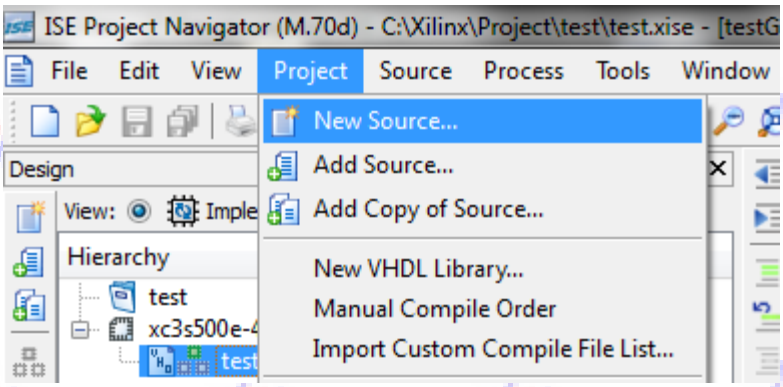
# XILINX ISE - PART 2
# Write a VHDL source




**Create a new Source**

Select : Project -> New Source

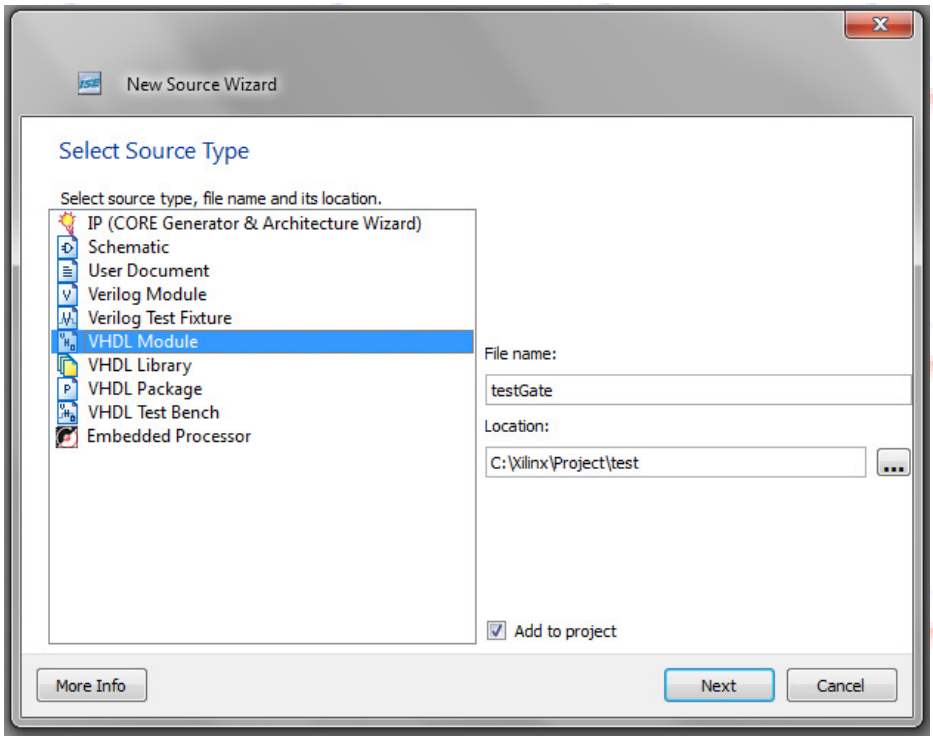
**Create a new Source**

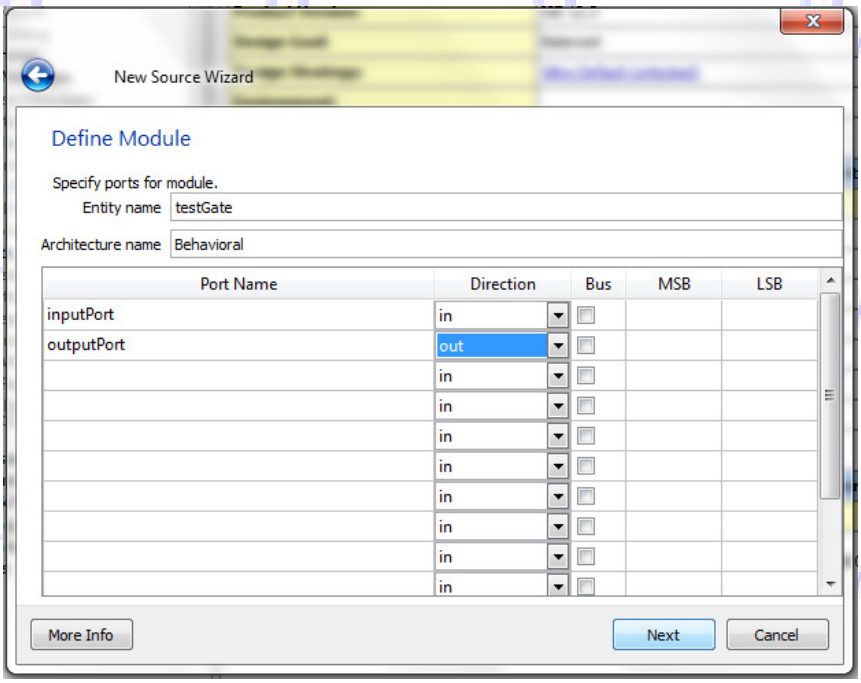
Select VHDL Module

Choose your file name
Here : "testGate"

Check "Add to project"

Click on "**Next**"






**Create a new Source**

This window helps you to create your module interface. It will generate the VHDL code of your interface.

In our case we will create an interface with :

- 1 input port : “inputPort”
- 1 output port : “outputPort”

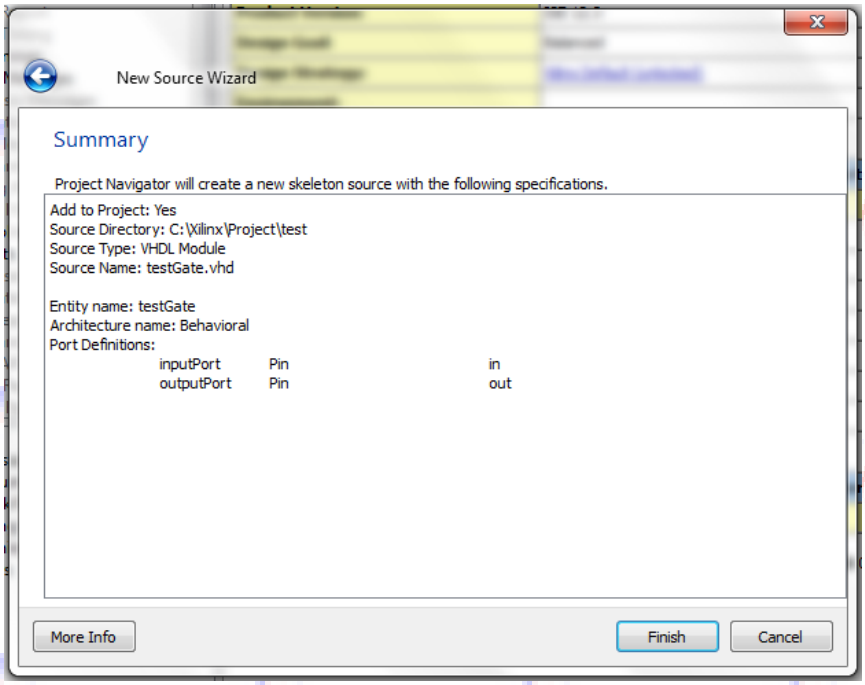
Select “in” direction for inputPort
Select “out” direction for outputPort

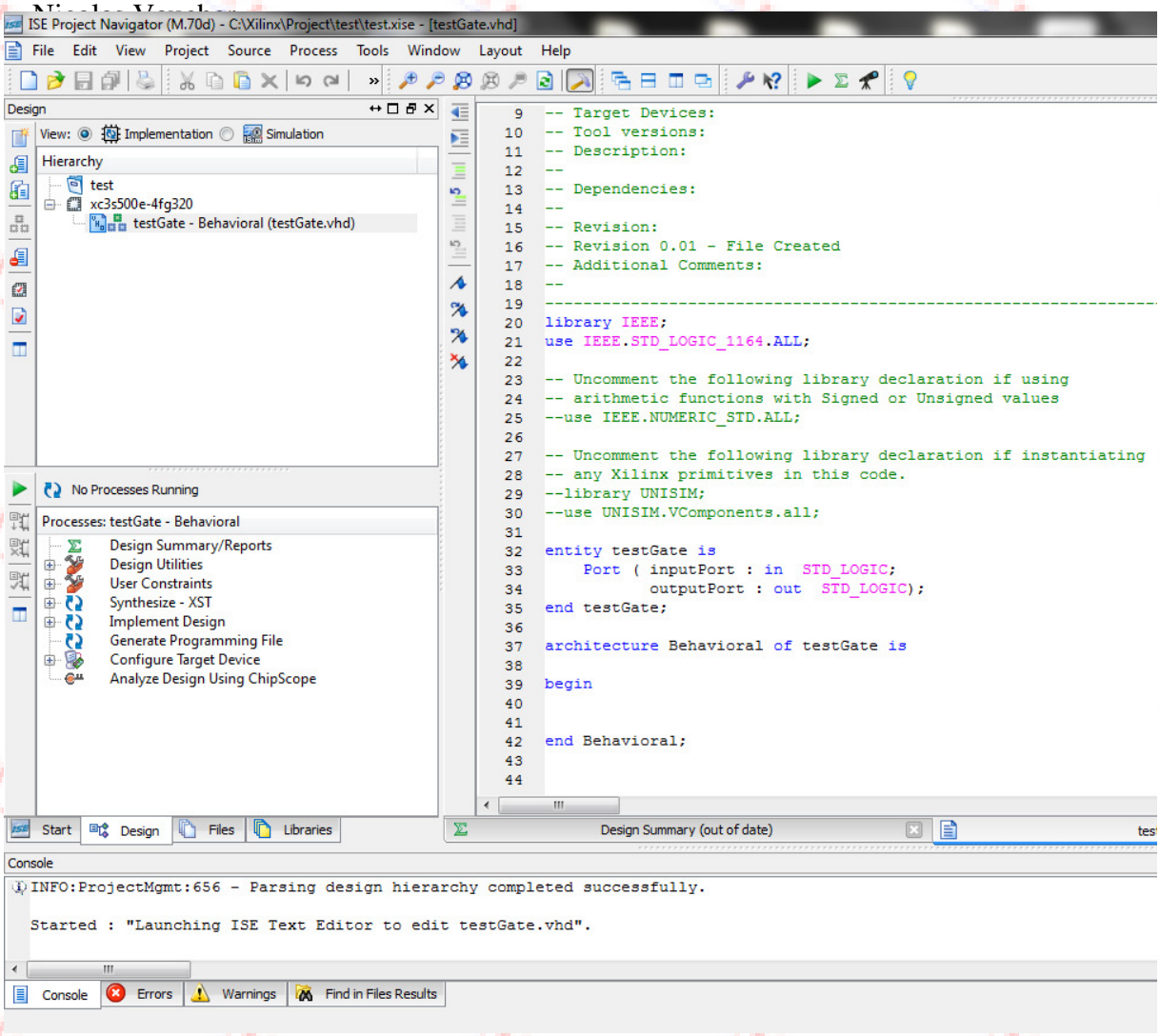
Click on “**Next**”

**Create a new Source**

A Summary window will show the parameters of your VHDL module skeleton.

Click on “**Finish**”






The Xilinx tool has generated your VHDL module skeleton. It includes:

- The Libraries :

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
```

- The entity declaration:

```
entity testGate is
    Port ( inputPort : in  STD_LOGIC;
           outputPort : out  STD_LOGIC);
end testGate;
```

- An empty architecture:

```
architecture Behavioral of testGate is

begin


end Behavioral;
```

We have to change the Libraries by:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
```

We will fill the architecture by:

```
outputPort <= not inputPort;
```

The complete file should be:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity testGate is
    Port ( inputPort : in  STD_LOGIC;
           outputPort : out  STD_LOGIC);
end testGate;

architecture Behavioral of testGate is

begin

outputPort <= not inputPort;

end Behavioral;
```

Save your file by pressing **ctrl-S.**