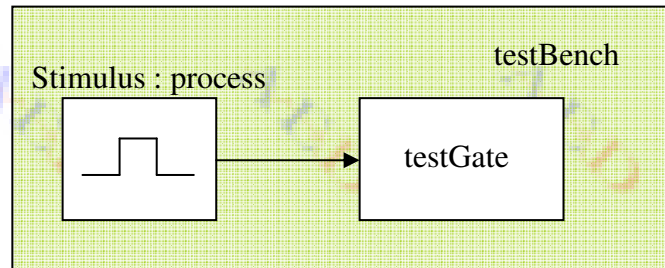


## XILINX ISE - PART 3

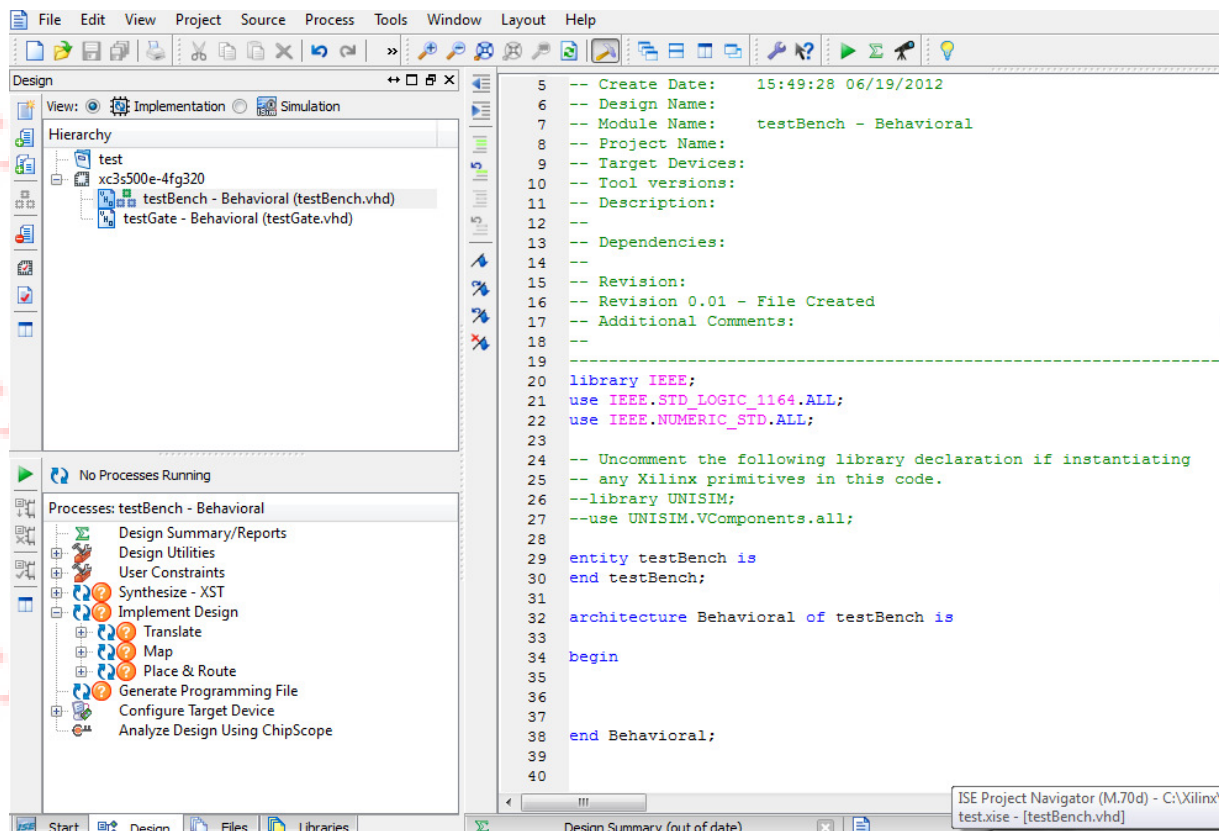
### Write a test bench

We want to simulate the architecture of testGate (written in part 2). We have to create a new VHDL source which will generate stimulus on the input signals of testGate.

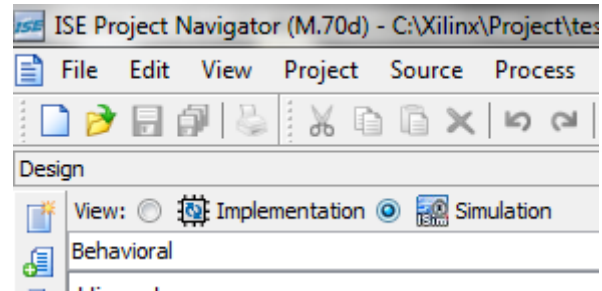


First create a new VHDL Module (part 2) with :  
Name = testBench  
Interface : empty

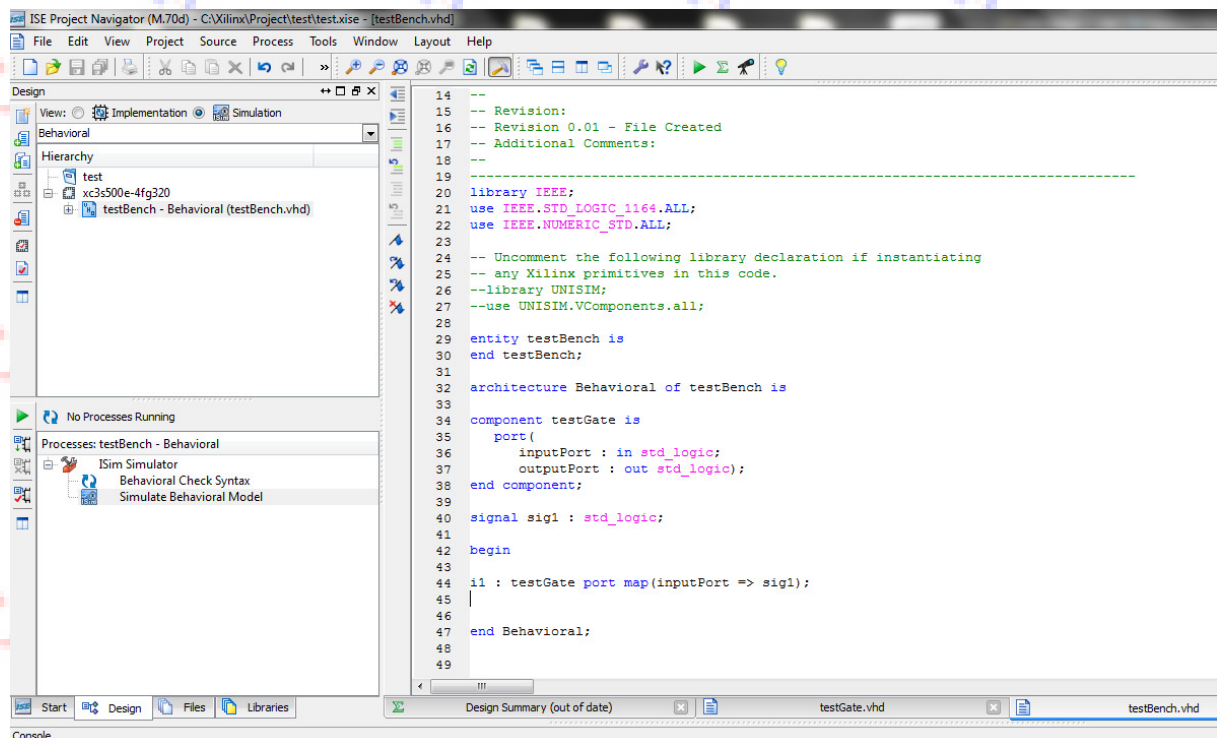
You should have the following result:



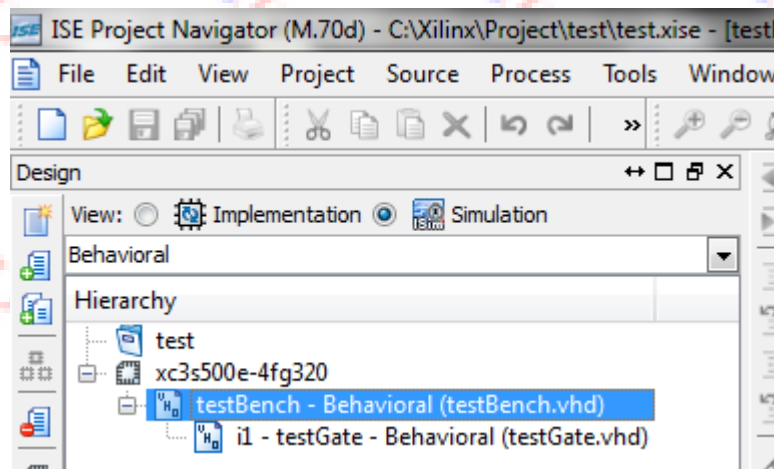
Select the simulation mode by clicking on the “simulation” button:



Now we have to instantiate the testGate module in the testBench. We will use the structural description to do this. The testBench will look like to:



Now testBench instantiate testGate. Note that the module testGate is UNDER the testBench module:



The instance name of the module testGate is “i1”.

Now testBench module uses the testGate module but do nothing. The testBench module have to stimulate the input signals of testGate in order to check the behaviour of the architecture. testGate has only one input port : “inputPort”. We create a signal “sig1” that will be connected to “inputPort” of testGate. We are going to use a process to generate a specific pattern on “sig1”:

```
stimulus : process
begin
    sig1 <= '0';
    wait for 100ns;
    sig1 <= '1';
    wait for 100ns;
    sig1 <= '0';
    wait for 100ns;
    sig1 <= '1';
    wait for 100ns;
end process;
```

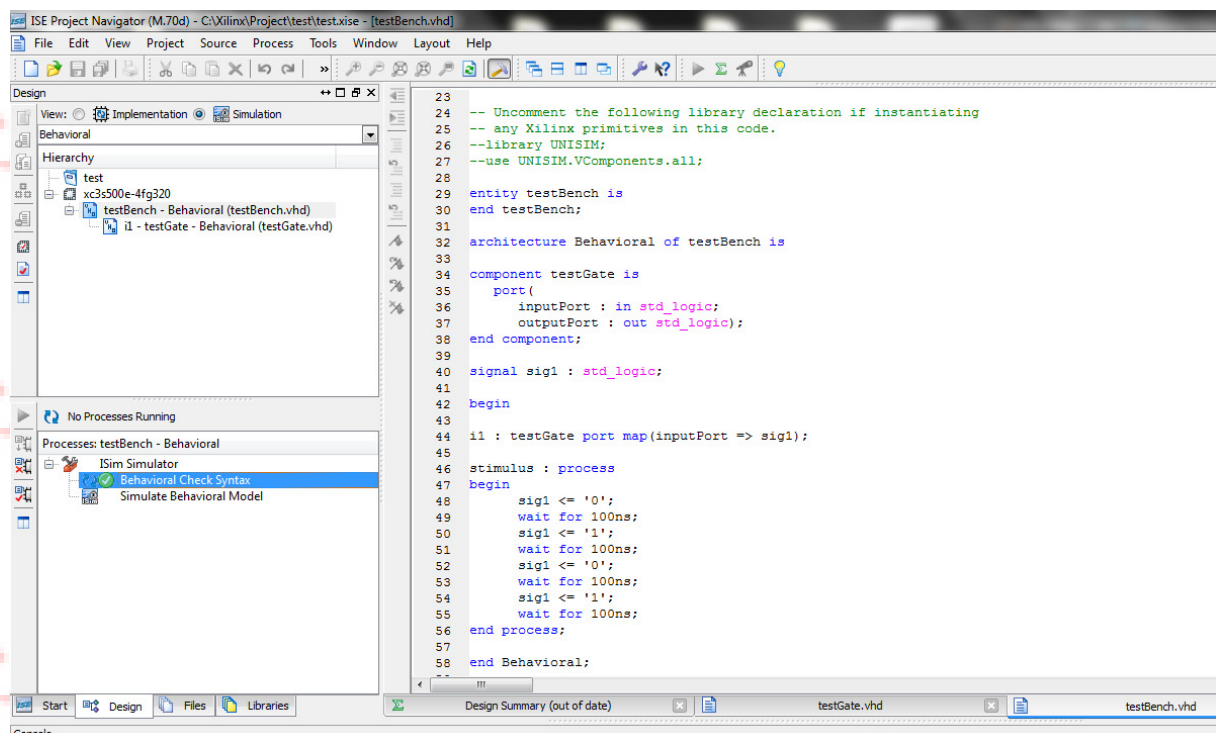
This process has no sensivity list because it must start immediately and must restart when the end is reached.

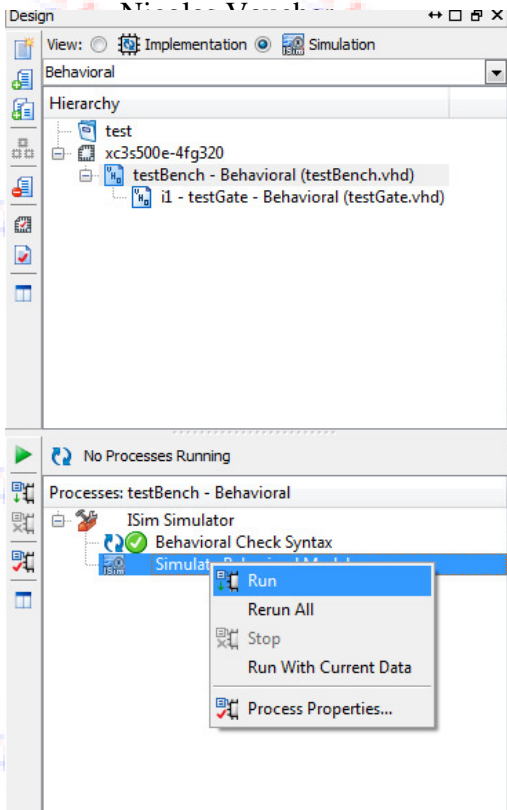
The name of the process is “stimulus”. You can give the name you want to the process.

The ‘0’ value will be immediately given to the signal “sig1”. After, the process will update the signal value and “wait 100ns”

After 100ns, the ‘1’ value will be given to the signal “sig1” and the wait instruction will update the signal and wait for 100ns. Etc...

When the process reach the “end process” instruction, it restarts immediately because there is no sensivity list.





To simulate the design, you have to select the testBench module (left click on testBench in the upper left window) and right click on “simulate behavioural model” in the lower right window to open the menu.

Select “run” or “rerun all” to launch the simulation tool Isim.

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