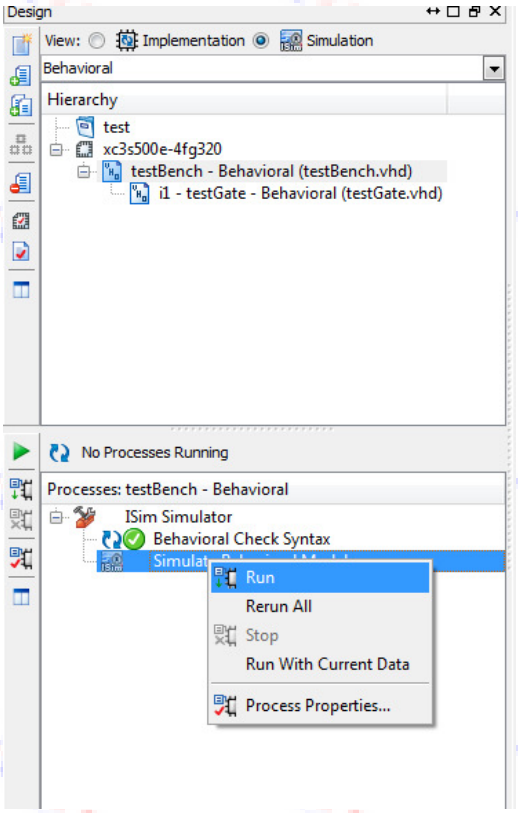
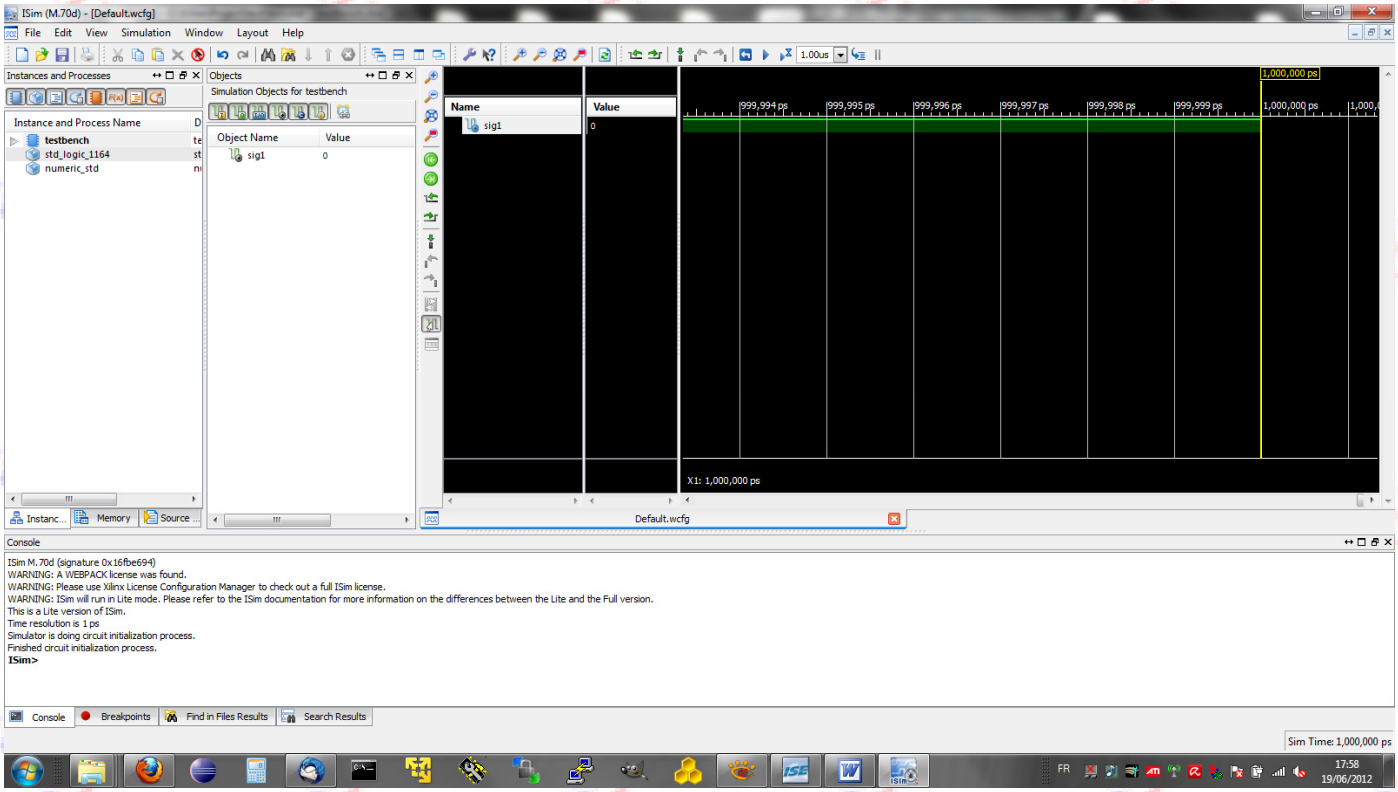
XILINX ISE - PART 4
Simulation

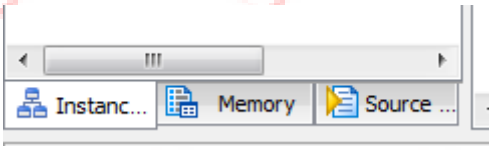


To simulate the design, you have to select the testBench module (left click on testBench in the upper left window) and right click on “simulate behavioural model” in the lower right window to open the menu.

Select “run” or “rerun all” to launch the simulation tool ISim.

ISIM

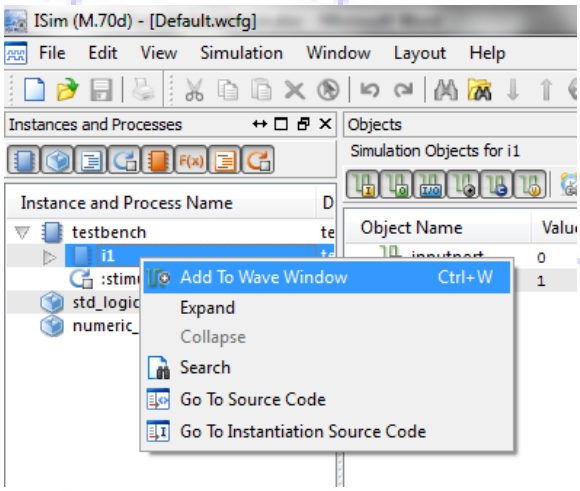


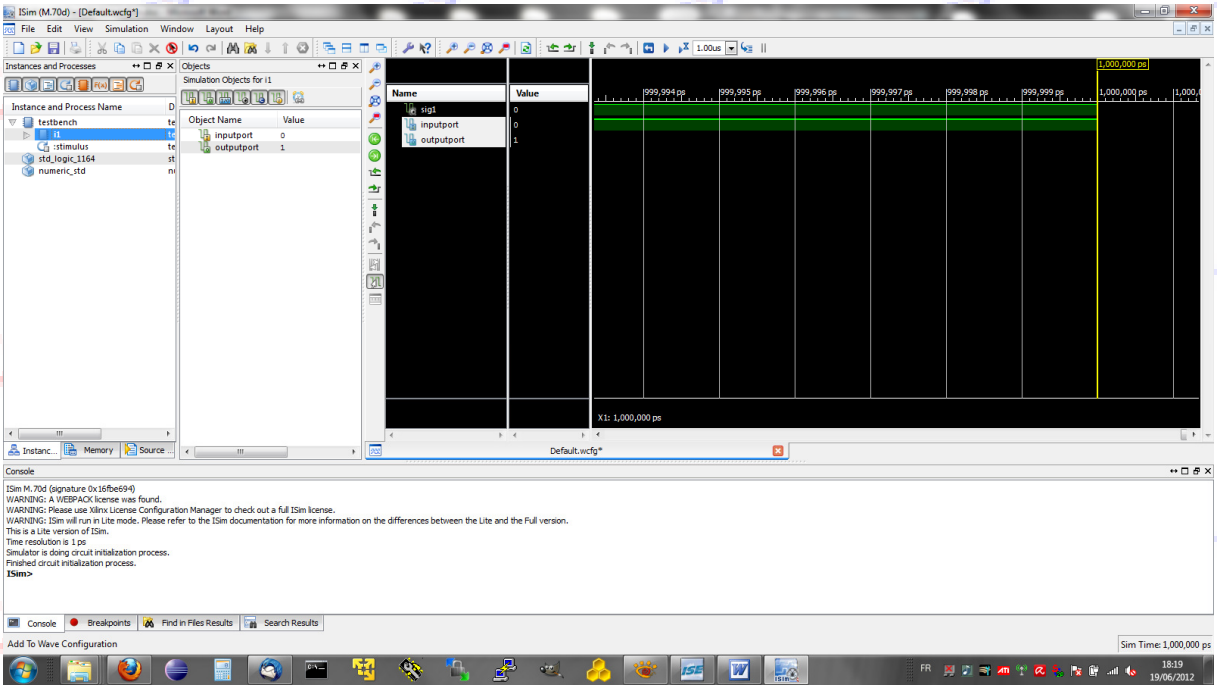


Select “Instance” at the bottom of the left window

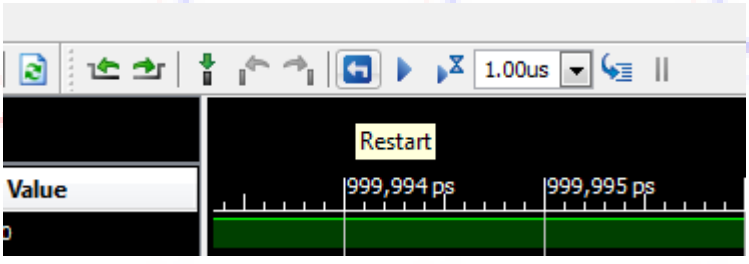
Add signals of the i1 instance in the wave window in order to view all the i1 signals (interface and internal signals).

- Open testBench
- right click on the “i1” instance
- select Add to wave window



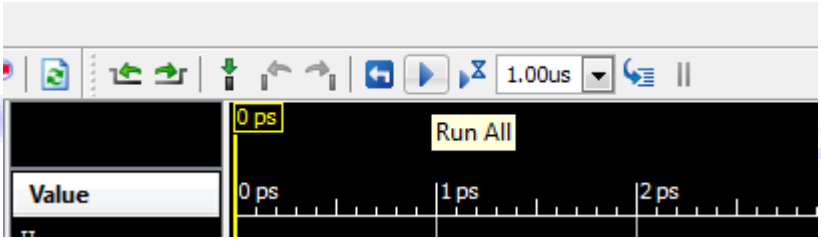


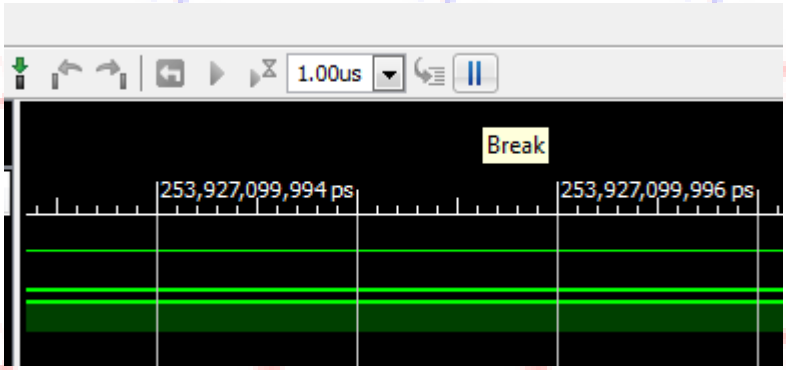
Signals inputPort and outputPort are now displayed in the wave window.



Click on “restart” icon in the tool bar. This action resets the simulator.

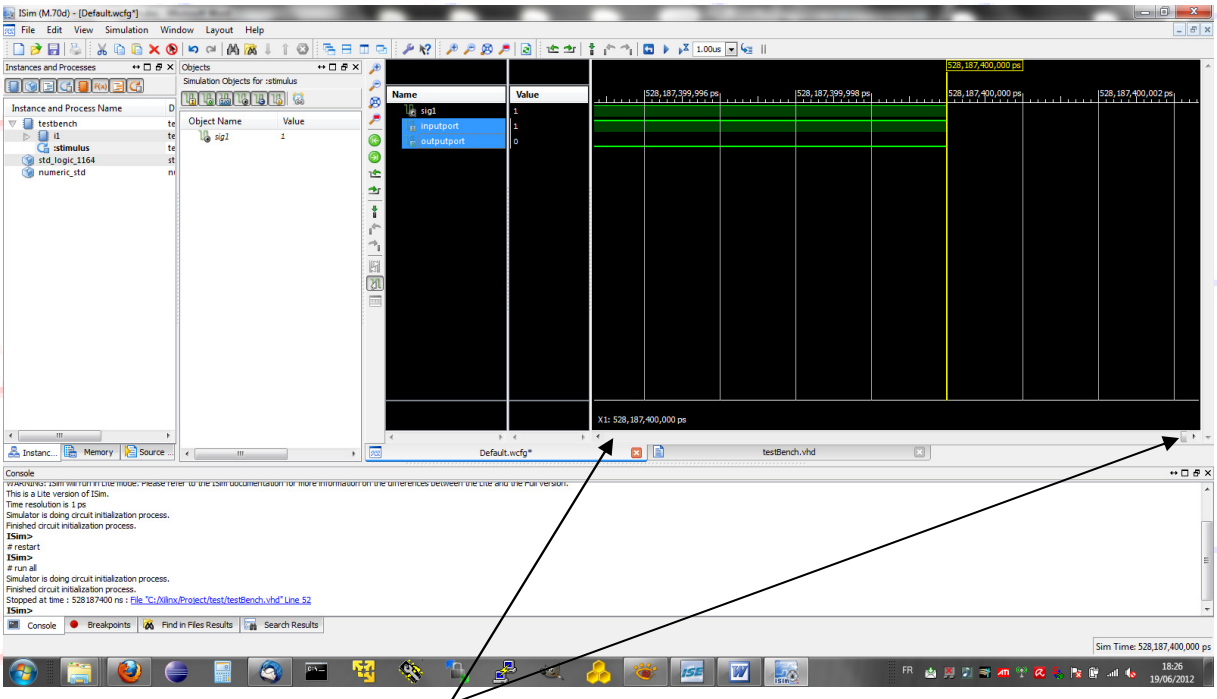
Click on “Run All” icon (in the tool bar) to start the simulation.



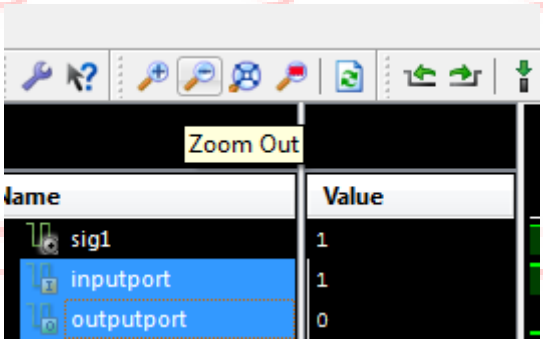


Click on “Break” icon (in the tool bar) to stop the simulation.

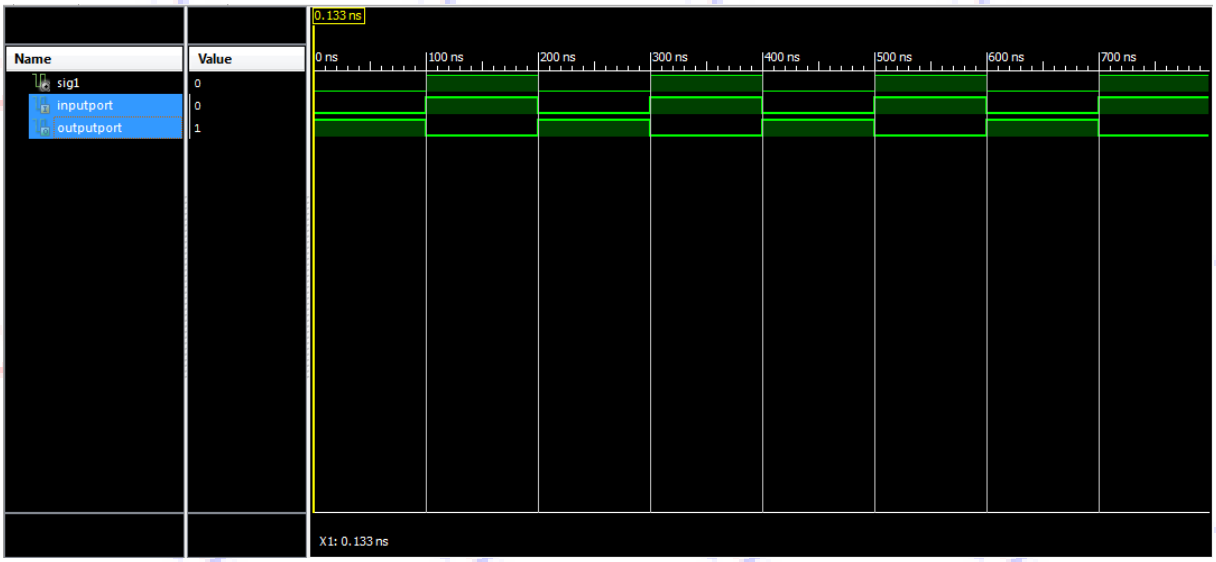
Select the “Default.wcfg” window to display the waveforms.



Move the cursor to the beginning of the simulation



Zoom out to see some waveforms.



It is now up to you to understand the waveforms:
At Time 0, inputPort is low (‘0’) and outputPort is high (‘1’).
At time 100ns, when inputPort goes high (‘1’), outputPort goes low (‘0’).
At time 200ns, when inputPort goes low (‘0’), outputPort goes high (‘1’).

The relation between inputPort and outputPort is an INVERSION.

$$\mathbf{outputPort=\overline{inputPort}}$$

This is described in the VHDL testGate module by:

outputPort <= not inputPort;