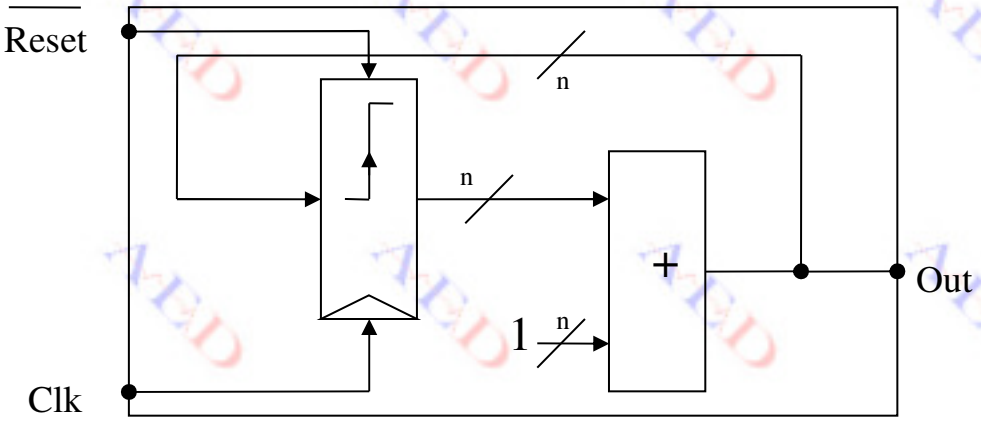
VHDL Architecture
Counter example

(During this training use only the dataflow description)



Level 1:

1. Implements this model with VHDL dataflow instructions.
2. Simulate this model with n=8
   a. What happens when reset=1 and reset=0
   b. What is the minimum value and the maximum value (in hex)?
3. Implement this model with n=26. Assign pins CLK to 50MHz external clock, reset to a switch and out[25] to a LED
   a. What is the Led behaviour? Explain.
   b. What is it frequency? Explain.

Level 2:

1. Modify (add the necessary hardware to) the architecture to :
   a. create a counter which counts from 0 to N. When it reaches N it will restart to 0.
2. Draw the schematic.
3. Translate the schematic in dataflow description.
4. Simulate and validate

Level 3:

1. Modify (add the necessary hardware to) the architecture to :
   a. create a counter which counts from 0 to N. When it reaches N it will restart to 0.
   b. Add a signal “Enable” which lets counter runs when equal to 1 and freezes the counter when equal to 0.
2. Draw the schematic.

3. Translate the schematic in dataflow description.
4. Simulate and validate

Level 4:

1. Always in Dataflow description: One counter (Counter1) will be used to count from 0 to N. This counter increment on each rising edge of the clock. A second counter (Counter2) will be used to count from 0 to M. This counter will increment on clock rising edge AND when the Counter1 reaches N.