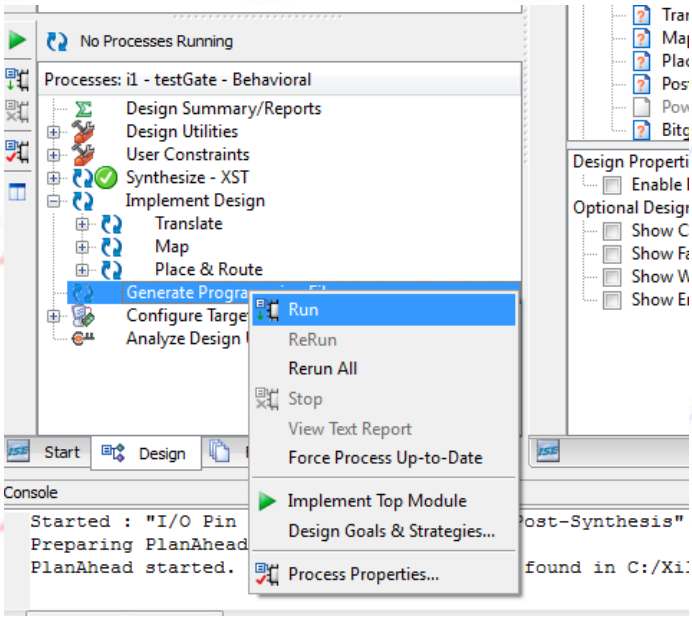
XILINX ISE - PART 6
Synthesis

Your design is ready to be synthesised.

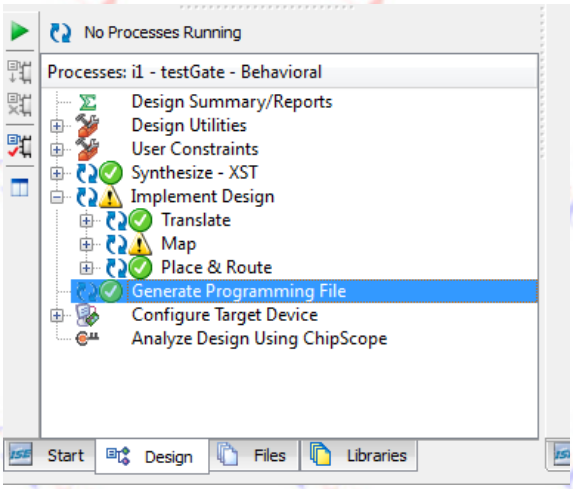


Launch the full process of :

- Synthesis
- Implement Design
  - Place
  - Route
- Generate bit stream file

By right clicking on “Generate Programming File” and select “Run”

All tools (synthesis, place and route, etc.) will be launched automatically. This process can take several minutes….



When the process is finished, you must obtains some warning and green marks.

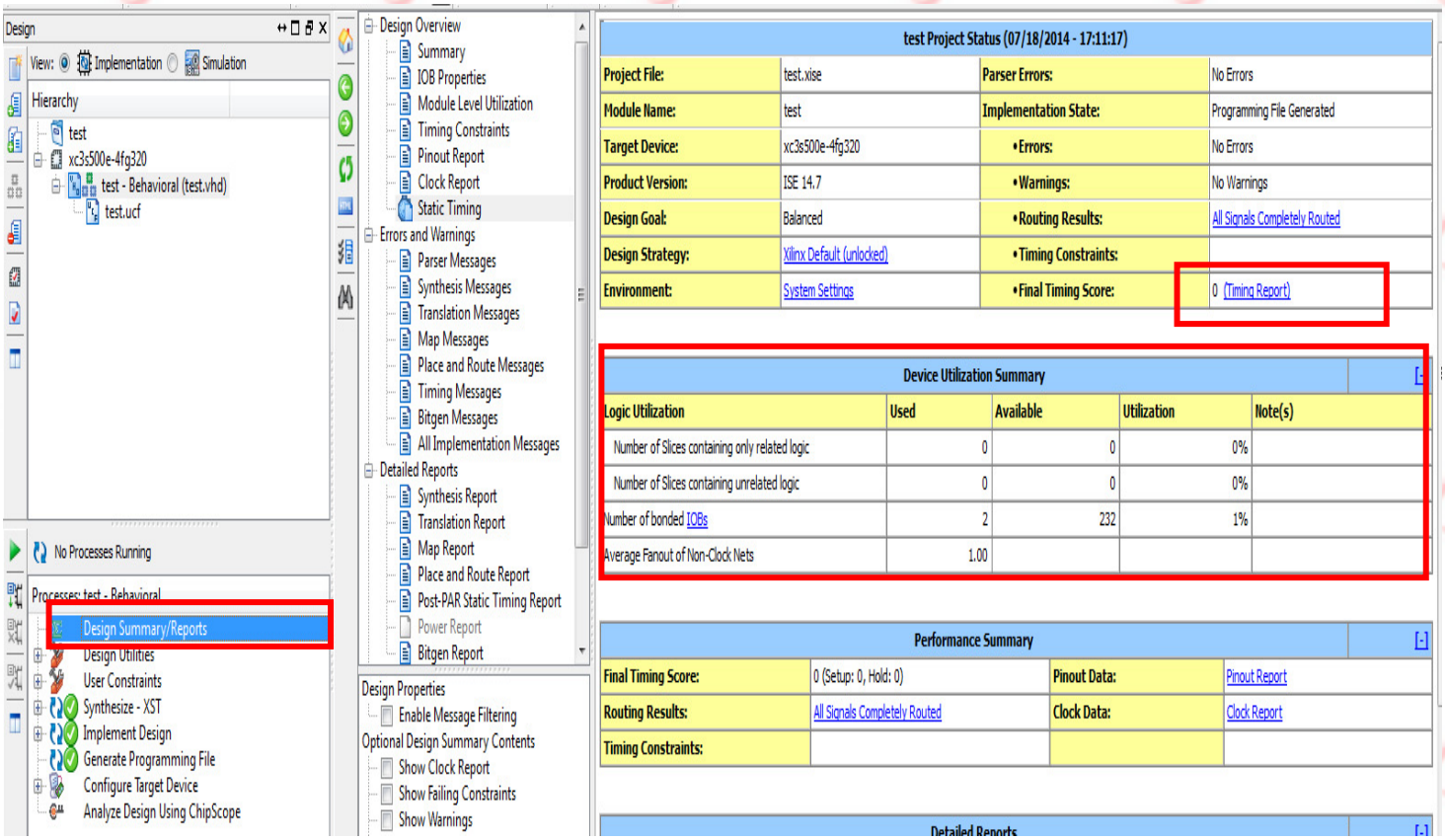
The process will be stopped if an error is detected in your design. In this case you have to correct your error and restart the process (and so on…).

When a design has been successfully generated, two information are very important:

- Used area : how much slices (or CLBs) does your design uses.
- Speed : what is the maximum (estimated) speed your design can reach.

You can find these information by double clicking on “Design Summary/Reports”.

In the “Device utilisation summary” array are displayed the number of IOs and slices your design is using.



To find the speed of your design, click on “Timings reports”

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Data Sheet report:
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All values displayed in nanoseconds (ns)

Pad to Pad
---------------+---------------+---------+
Source Pad     |Destination Pad|  Delay  |
---------------+---------------+---------+
inputPort      |outputPort     |    6.172|
---------------+---------------+---------+
```

In this case the signal takes 6.172 ns to goes from inputPort to outputPort.