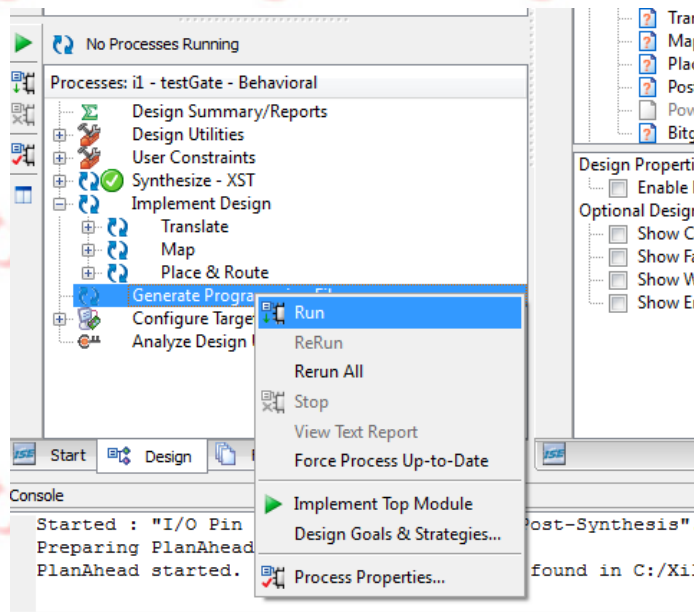


XILINX ISE - PART 6

Synthesis

Your design is ready to be synthesised.



Launch the full process of :

- Synthesis
- Implement Design
 - o Place
 - o Route
- Generate bit stream file

By right clicking on “Generate Programming File” and select “Run”

All tools (synthesis, place and route, etc.) will be launched automatically. This process can take several minutes....

When the process is finished, you must obtain some warning and green marks.

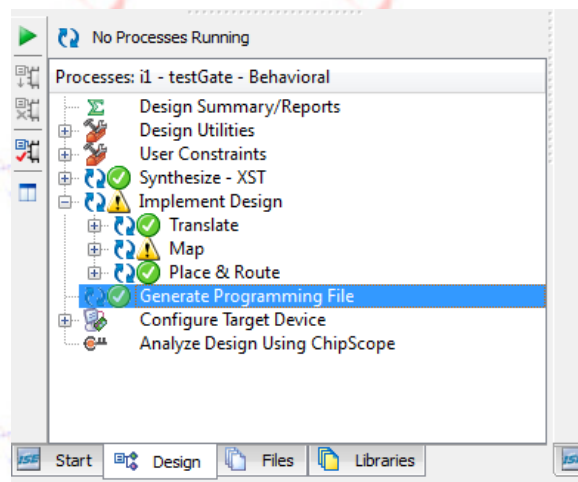
The process will be stopped if an error is detected in your design. In this case you have to correct your error and restart the process (and so on...).

When a design has been successfully generated, two information are very important:

- Used area : how much slices (or CLBs) does your design uses.
- Speed : what is the maximum (estimated) speed your design can reach.

You can find these information by double clicking on “Design Summary/Reports”.

In the “Device utilisation summary” array are displayed the number of IOs and slices your design is using.



The screenshot shows the Xilinx ISE software interface. The 'test Project Status (07/18/2014 - 17:11:17)' window is open, displaying project details. The 'Final Timing Score' is highlighted with a red box, showing '0 (Timing Report)'. Below it, the 'Device Utilization Summary' table is also highlighted with a red box. The 'Performance Summary' table shows 'Final Timing Score: 0 (Setup: 0, Hold: 0)'. The 'Design Overview' pane on the left shows a tree view of reports, with 'Design Summary/Reports' highlighted in red.

test Project Status (07/18/2014 - 17:11:17)			
Project File:	test.xise	Parser Errors:	No Errors
Module Name:	test	Implementation State:	Programming File Generated
Target Device:	xc3s500e-4fg320	•Errors:	No Errors
Product Version:	ISE 14.7	•Warnings:	No Warnings
Design Goal:	Balanced	•Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	0 (Timing Report)

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	
Number of bonded IOBs	2	232	1%	
Average Fanout of Non-Clock Nets	1.00			

Performance Summary			
Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:			

To find the speed of your design, click on “Timings reports”

Data Sheet report:

All values displayed in nanoseconds (ns)

Pad to Pad

Source Pad	Destination Pad	Delay
inputPort	outputPort	6.172

In this case the signal takes 6.172 ns to goes from inputPort to outputPort.