

# Advanced Electronic Design



## IEEE 754 Floating Point Unit

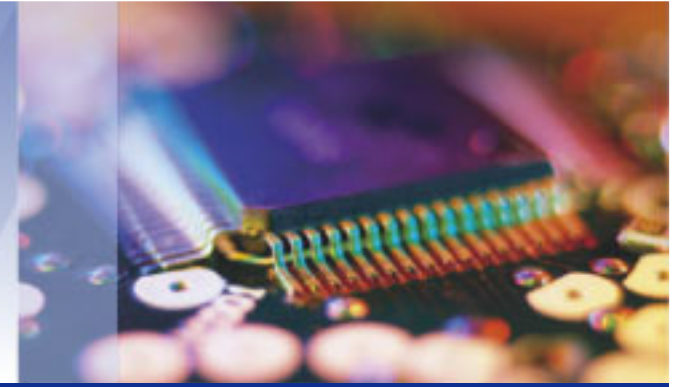
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# Arithmetic Unit

## Features



- **IEEE-754 floating point operators**

Adder, Multiplier, Divider, Remainder, Square root, Conversions, Tests  
Single and double precision (32 and 64 bits)

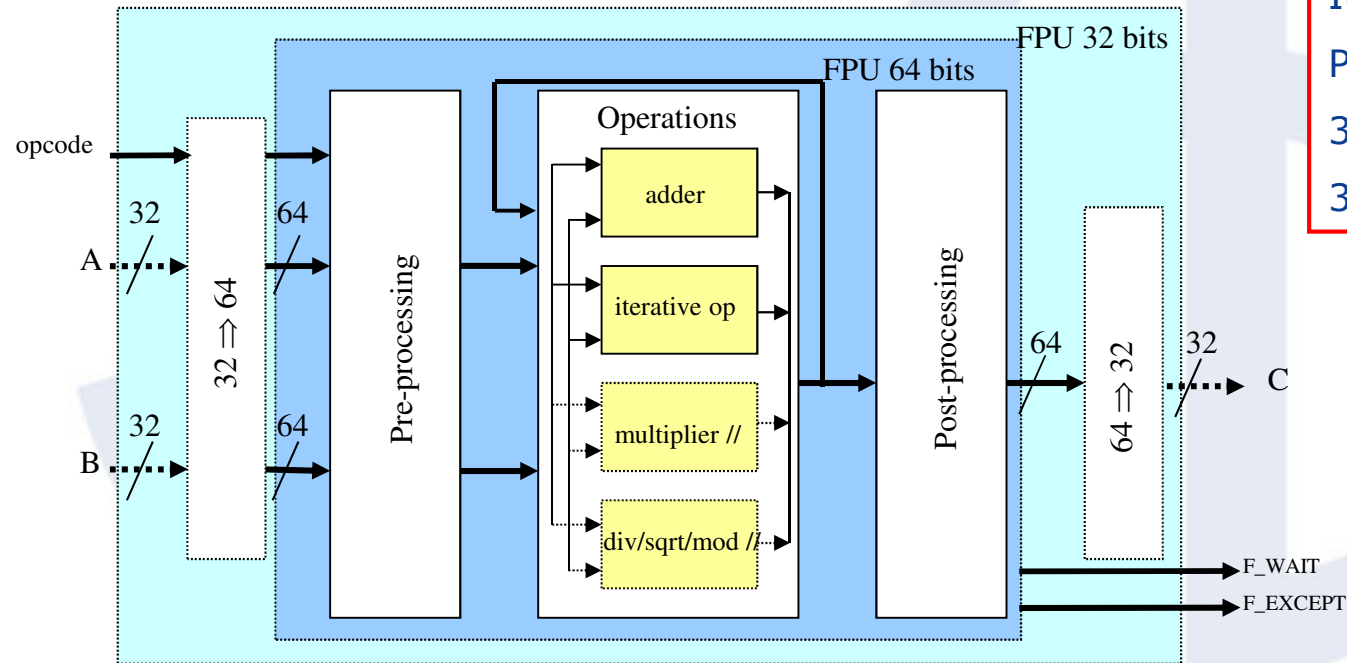
- **Integer operators**

Adder, Multiplier, Divider, Remainder, Conversions, Tests  
32 and 64 bits of precision (int and long type)

- **3 pipeline stages**

# Arithmetic Unit

## Architecture



- 64 bits operator size
- Iterative operators
- Parallel operators
- 32 or 64 bits interface
- 3 pipeline stages

# Arithmetic Unit

## Operators features



IEEE-754 Floating point operations	
Operations	Cycle number
Add, Sub, Mul, Neg, Test (Float and Double)	1
Divider, <b>Square root</b> (Float)	1-27
Divider, <b>Square root</b> (Double)	1-56
Remainder, Fmod (Float)	1-276
Remainder, Fmod (Double)	1-2097
Convert (i2f, i2d, l2f, l2d, f2i, f2l, d2i, d2l, f2d, d2f, cast)	1
Ceil, Floor, Rint (Float and Double)	1
Abs, Min, Max (Float and Double)	1

Integer operations	
Operations	Cycle number
Add, Sub, Mul, Neg, Test (Int and Long)	1
Divider (Int)	1-32
Divider (Long)	1-64
Remainder (Int)	1-32
Remainder (Long)	1-64
Abs, Min, Max (Int and Long)	1

Status	
Operations	Cycle number
Read status	1
Write status	1

**30 000 gates**

**250MHz for 90nm Technology**



# Arithmetic Unit



## ■ **FPU is used**

With LEON2 processor for spatial applications (FPGA/ASIC)

With T805 processor for spatial applications (FPGA/ASIC)

With JAP processor for military/industrial applications (FPGA)  
in last generation of french satellites

## ■ **Technology**

FPU has been mapped/tested for 90nm technology and several FPGAs (Actel, Xilinx, Altera, Lattice).

## ■ **IEEE 754 compatibility**

IEEE 754 compatibility 100% tested (including rounding modes/exceptions/denormalised numbers)

# Arithmetic Unit

## Contact

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